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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/517,518	03/02/2000	Jacques Wong	52352-317	4862

20277 7590 12/07/2001

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EXAMINER
THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/07/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/517,518	Applicant(s) WONG ET AL.	
	Examiner A. M. Thompson	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This application has been examined. Claims 1-9 are pending.

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to: At Figure 4, #62, the writing extends outside box boundaries. At Fig. 66, spell out "Req'ts"; at Figure 78, spell out "T-L". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Fig. 2, reference characters 28, 30, 32 and 34 are respectively used to designate different sub-modules. Applicant may either give each sub-module its own reference number or enclose the sub-modules pertaining to a particular stage in a box and label that box with one number. Figure 4 is similarly objected to because reference characters 64, 65, 66, and 68 are respectively used to designate different sub-modules. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: In the Abstract at line 3, for grammatical purposes, insert article - -the- - after "using" or rephrase in some other manner. Appropriate correction is required.

Claim Objections

5. Claims 1 and 5 are objected to because of the following informalities: Pursuant to claim 1, at line 3, use plural of "module". At line 6, pluralize "module". At line 5, insert semicolon (;) after "system". Pursuant to claim 5, at line 1, pluralize "include". Pursuant to claim 7, at line 2, delete "for verifying" and insert - -to verify- -for grammatical clarity. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Rejection of Claims 1-4 and 6-9

7. Claims 1-4 and 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Dupenloup, U.S. Patent 6,295,636. Dupenloup teaches RTL analysis for improved logic synthesis which involves synthesizing integrated circuit designs in RTL level descriptions into gate level description.

7.1 Pursuant to claim 1 which recites [a] method of synthesizing a register transfer level based design of a system (col. 3, ll. 20-23 discloses that one object of the

invention is to define tools that automatically extract from RTL code design information required for synthesis. Additionally, col. 4, ll. 28-32 discloses that the invention is a method to synthesize IC designs in RTL descriptions into gate level descriptions) comprising the steps of determining sub modules of a top level system: col. 4, ll. 4-7 discloses that this determination is done via a dc_shell command; additionally, Figs. 14 and 16 illustrate design sub-modules;

determining individual time budgets for each sub-module based on timing requirements of the top-level system: Dupenloup discloses the use of time budgets at col. 42, ll. 29-31; col. 16, lines 6-8; col. 43, line 29 to col. 44, line 20; see also col. 43, ll. 15-18;

synthesizing gate-level designs of the sub-module based on the determined time budgets for the individual sub-modules: Fig. 19 illustrates synthesis based on time budget requirements; see also col. 43, ll. 15-25; col. 1, ll. 34-35 discloses that RTL code is *synthesized* to generate a gate level design or netlist i.e. the process of synthesis produces a gate level netlist; see also col. 67, ll. 1-11;

integrating the gate level designs of the individual sub-modules to form a top level design: Fig. 14 illustrates the integration of sub-modules to form a top level design; see also col. 41, ll. 1-13;

testing the top-level design for conformance with top level design requirements: see Fig. 19 wherein the top level design requirements are the constraints; col. 43, 42, line 63 to col. 43, line 25 also indicates a process of iterative improvement involving the

top-level constraint until all constraints are met. In order to know whether all constraints are met implies the presence of a testing requirement;

generating a top-level netlist when the top-level design conforms to the top-level design requirements: Fig. 19, #456 illustrates the generation of a final netlist.

7.2 Pursuant to claim 2, further comprising generating gate-level netlists for the gate-level designs of each of the sub-modules: col. 49, line 51 to col. 50, line 31 teaches the progressive *synthesis* of sub-module.

7.3 Pursuant to claim 3 wherein the step of integrating the gate-level designs includes integrating the gate–level netlists of the sub-modules: Fig. 14, #394.

7.4 Pursuant to claim 4, further comprising testing the gate-level designs for conformance with gate-level design requirements of the individual sub-modules prior to integrating the gate-level designs to form the top-level design: see Fig. 14 and Fig. 19 which details the synthesis process applicable to the sub-modules; col. 42, ll. 10-31, col. 43, ll. 8-25,.

7.5 Pursuant to claim 6, wherein the gate-level netlists are generated for sub-modules only if the timing requirements for the individual sub-modules are met: col. 71, ll. 9-23 discloses this process of synthesis for each individual sub-module.

7.6 Pursuant to claim 7, wherein the step of synthesizing is re-performed and the gate-level designs are re-tested in an iterative manner for verifying conformance of the gate-level designs with the timing requirements of the individual sub-modules: Figure 19 illustrates this limitation; see also col. 43, ll. 3-25.

7.7 Pursuant to claim 8, wherein the step of synthesizing gate-level designs is further based on wire-loads and input/output loads/drivers: col. 42, ll. 10-28 discloses that default constraints involving values for input delay, output loading, and output delay are set on the I/O ports of modules; col. 41, ll. 49-52 discloses that the major synthesis constraints propagated by characterization include among other things wire load modules; see also Fig. 15 and 17.

7.8 Pursuant to claim 9, wherein the step of verifying conformance of the gate-level designs includes performing dynamic simulations on the gate-level designs: col. 10, ll. 33-51.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claim 5

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dupenloup, U.S. Patent 6,295,636. Dupenloup discloses RTL analysis method for improved logic synthesis. Although Dupenloup does not explicitly state that a static timing analysis is performed, Dupenloup suggests the use of static timing analysis on individual sub-modules in disclosing motivations for identifying clock domains and clock domain interfaces. Furthermore, Fig. 3a-3c display the clock domains and one of

ordinary skill in the art could classify them as sub-modules because these domains are just one of many modules needed for a particular integrated circuit.

9.1 Pursuant to claim 5, wherein testing the gate-level designs include performing static timing analysis on the individual sub-modules for conformance with timing requirements for the individual sub-blocks: col. 11, line 55 to col. 12, line 42 and col. 13, ll. 33-36.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please refer to the PTO-892.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m..

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323. The general fax phone number for the organization where this application is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

12. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
November 30, 2001

VUTHE SIEK
Patent Examiner